CLAIMS

1. An apparatus for driving a plurality of display units in a mobile electronic apparatus, each including a plurality of data lines, a plurality of scan line and a plurality of pixels each provided at one of said data lines and one of said scan lines, comprising:

at least one of a common data driver circuit and a common scan driver circuit,

said common data driver circuit including a plurality of first switch groups, each first switch group being connected to the data lines of one of said display units for driving the data lines of said one of said display units,

said common scan driver circuit including a plurality of second switch groups, each second switch group being connected to the scan lines of one of said display units for driving the scan lines of said one of said display units.

2. The apparatus as set forth in claim 1, wherein said common data driver circuit comprises:

a plurality of frame memories for storing video signals, each for one of said display units;

a plurality of third switch groups each group being connected to one of said frame memories and being operated in synchronization with operations of said first switch groups;

a line memory, connected to said third switch groups, for selectively storing one line data of said frame memories in accordance with the operations of said third switch groups;

a gradation voltage generating circuit;

a decoder circuit, connected to said line memory and said gradation voltage generating circuit, for selecting gradation voltages from said gradation voltage

generating circuit in accordance with output signals of said line memory; and

an output circuit, connected between said decoder circuit and said first switch groups, for transmitting said selected gradation voltages to said first switch groups, so that said selected gradation voltages are transmitted to the data lines of one of said display units in accordance with the operations of said first switch groups.

3. The apparatus as set forth in claim 2, wherein said gradation voltage generating circuit comprises a plurality of gradation voltage generating units each for one of said display units.

4. The apparatus as set forth in claim 2, wherein said output comprises:

a plurality of voltage followers, connected to said decoder circuit, for amplifying said selected gradation voltages;

a plurality of first switches each connected to one of said voltage followers; and

a plurality of second switches each connected between an input of one of said voltage followers and an output of one of said first switches,

wherein said first switches are turned ON for a first predetermined time period, and then, said second switches are turned ON while said first switches are turned OFF.

5. The apparatus as set forth in claim 4, wherein said output circuit further comprises a plurality of third switches each connected between the output of one of said first switches and a ground, said third switches being turned ON by a control signal when driving of one of said display units is switched to driving of the other of said display units.

6. The apparatus as set forth in claim 1, wherein said

common data driver circuit comprises:

a shift register circuit for shifting a horizontal start signal in accordance with a horizontal clock signal;

a line memory, connected to said shift register circuit, for storing one line data in accordance with said shift register circuit;

a gradation voltage generating circuit;

a decoder circuit, connected to said line memory and said gradation voltage generating circuit, for selecting gradation voltages from said gradation voltage generating circuit in accordance with output signals of said line memory; and

an output circuit, connected between said decoder circuit and said first switch groups, for transmitting said selected gradation voltages to said first switch groups, so that said selected gradation voltages are transmitted to the data lines of one of said display units in accordance with the operations of said first switch groups.

7. The apparatus as set forth in claim 6, wherein said gradation voltage generating circuit comprises a plurality of gradation voltage generating units each for one of said display units.

8. The apparatus as set forth in claim 6, wherein said output circuit comprises:

a plurality of voltage followers, connected to said decoder circuit, for amplifying said selected gradation voltages;

a plurality of first switches each connected to one of said voltage followers; and

a plurality of second switches each connected between an input of one of said voltage followers and an output of one of said first switches,

wherein said first switches are turned ON for a first predetermined time period, and then, said second switches are turned ON while said first switches are turned OFF.

9. The apparatus as set forth in claim 8, wherein said output circuit further comprises a plurality of third switches each connected between the output of one of said first switches and a ground, said third switches being turned ON by a control signal when driving of one of said display units is switched to driving of the other of said display units.

10. The apparatus as set forth in claim 1, wherein said scan driver circuit comprises:

a shift register circuit for shifting a vertical start signal in accordance with a vertical clock signal; and

an output circuit, connected to said shift register circuit, for transmitting output signals of said shift register circuit to said second switch groups, so that the scan lines of one of said display units are sequentially scanned by said second switch groups.

11. The apparatus as set forth in claim 1, wherein said scan driver circuit further includes a plurality of fourth switch groups each fourth switch group being connected to the scan lines of said display units for supplying an off-level voltage to the scan lines of said one of said display units.

12. The apparatus as set forth in claim 1, further comprising:

an oscillator;

a plurality of first frequency dividers, connected to said oscillator, for frequency-dividing an output signal of said oscillator to generate horizontal clock signals;

a fifth switch group connected to said first

frequency dividers;

a plurality of second frequency dividers, connected to said oscillator, for frequency-dividing the output signal of said oscillator to generate vertical clock signals;

a sixth switch group connected to said second frequency dividers; and

a frequency control circuit, connected to said fifth and sixth switch groups, for selecting and turning ON one switch of said fifth switch group and one switch of said sixth switch group, so that the data lines of said one of said display units are driven by a selected one of said horizontal clock signals and the scan lines of said one of said display units are driven by a selected one of said vertical clock signals, thus always realizing a definite frame frequency of said one of said display units.

13. An apparatus for driving a plurality of display units in a mobile electronic apparatus, each including a plurality of data lines, a plurality of scan line and a plurality of pixels each provided at one of said data lines and said scan lines, comprising:

a single common data driver circuit including a plurality of first switch groups, each first switch group being connected to the data lines of one of said display units for driving the data lines of said one of said display units; and

a plurality of scan driver circuits, each connected to the scan lines of one of said display units, for driving the scan lines of said one of said display units.

14. The apparatus as set forth in claim 13, wherein said single common data driver circuit comprises:

a plurality of frame memories for storing video signals, each for one of said display units;

a plurality of third switch groups each group being connected to one of said frame memories and being operated in synchronization with operations of said first switch groups;

a line memory, connected to said third switch groups, for selectively storing one line data of said frame memories in accordance with the operations of said third switch groups;

a gradation voltage generating circuit;

a decoder circuit, connected to said line memory and said gradation voltage generating circuit, for selecting gradation voltages from said gradation voltage generating circuit in accordance with output signals of said line memory; and

an output circuit, connected between said decoder circuit and said first switch groups, for transmitting said selected gradation voltages to said first switch groups, so that said selected gradation voltages are transmitted to the data lines of one of said display units in accordance with the operations of said first switch groups.

15. The apparatus as set forth in claim 14, wherein said gradation voltage generating circuit comprises a plurality of gradation voltage generating units each for one of said display units.

16. The apparatus as set forth in claim 14, wherein said output circuit comprises:

a plurality of voltage followers, connected to said decoder circuit, for amplifying said selected gradation voltages;

a plurality of first switches each connected to one of said voltage followers; and

a plurality of second switches each connected between an input of one of said voltage followers and an output

of one of said first switches,

wherein said first switches are turned ON for a first predetermined time period, and then, said second switches are turned ON while said first switches are turned OFF.

17. The apparatus as set forth in claim 16, wherein said output circuit further comprises a plurality of third switches each connected between the output of one of said first switches and a ground, said third switches being turned ON by a control signal when driving of one of said display units is switched to driving of the other of said display units.

18. The apparatus as set forth in claim 13, wherein said single common data driver circuit comprises:

a shift register circuit for shifting a horizontal start signal in accordance with a horizontal clock signal;

a line memory, connected to said shift register circuit, for storing one line data in accordance with said shift register circuit;

a gradation voltage generating circuit;

a decoder circuit, connected to said line memory and said gradation voltage generating circuit, for selecting gradation voltages from said gradation voltage generating circuit in accordance with output signals of said line memory; and

an output circuit, connected between said decoder circuit and said first switch groups, for transmitting said selected gradation voltages to said first switch groups, so that said selected gradation voltages are transmitted to the data lines of one of said display units in accordance with operations of said first switch groups.

19. The apparatus as set forth in claim 18, wherein said gradation voltage generating circuit comprises a plurality of

gradation voltage generating units each for one of said display units.

20. The apparatus as set forth in claim 18, wherein said output circuit comprises:

a plurality of voltage followers, connected to said decoder circuit, for amplifying said selected gradation voltages;

a plurality of first switches each connected to one of said voltage followers; and

a plurality of second switches each connected between an input of one of said voltage followers and an output of one of said first switches,

wherein said first switches are turned ON for a first predetermined time period, and then, said second switches are turned ON while said first switches are turned OFF.

21. The apparatus as set forth in claim 20, wherein said output circuit further comprises a plurality of third switches each connected between the output of one of said first switches and a ground, said third switches being turned ON by a control signal when driving of one of said display units is switched to driving of the other of said display units.

22. The apparatus as set forth in claim 13, wherein each of said scan driver circuits comprises:

a shift register circuit for shifting a vertical start signal in accordance with a vertical clock signal; and

an output circuit, connected to said shift register circuit, for transmitting output signals of said shift register circuit to said second switch sets, so that the scan lines of one of said display units are sequentially scanned by output signals of said output circuit.

23. The apparatus as set forth in claim 13, further

comprising:

an oscillator;

a plurality of first frequency dividers, connected to said oscillator, for frequency-dividing an output signal of said oscillator to generate horizontal clock signals;

a fourth switch group connected to said first frequency dividers;

a plurality of second frequency dividers, connected to said oscillator, for frequency-dividing the output signal of said oscillator to generate vertical clock signals;

a fifth switch group connected to said second frequency dividers; and

a frequency control circuit, connected to said fourth and fifth switch groups, for selecting and turning ON one switch of said fifth switch group and one switch of said fifth switch group, so that the data lines of said one of said display units are driven by a selected one of said horizontal clock signals and the scan lines of said one of said display units are driven by a selected one of said vertical clock signals, thus always realizing a definite frame frequency of said one of said display units.

24. An apparatus for driving a plurality of display units in a mobile electronic apparatus, each including a plurality of data lines, a plurality of scan line and a plurality of pixels each provided at one of said data lines and said scan lines, comprising:

a plurality of data driver circuits each connected to the data lines of one of said display units, for driving the data lines of said one of said display units;

a single common scan driver circuit including a plurality of first switch groups, each second switch group

being connected to the scan lines of one of said display units for driving the scan lines of said one of said display units.

25. The apparatus as set forth in claim 24, wherein each of said data driver circuits comprises:

a frame memory for storing video signals, for one of said display units;

a line memory, connected to said frame memory groups, for storing one line data of said frame memory;

a gradation voltage generating circuit;

a decoder circuit, connected to said line memory and said gradation voltage generating circuit, for selecting gradation voltages from said gradation voltage generating circuit in accordance with output signals of said line memory; and

an output circuit, connected to said decoder circuit, for outputting said selected gradation voltages, so that said selected gradation voltages are transmitted to the data lines of one of said display units.

26. The apparatus as set forth in claim 25, wherein said output circuit comprises:

a plurality of voltage followers, connected to said decoder circuit, for amplifying said selected gradation voltages;

a plurality of first switches each connected to one of said voltage followers; and

a plurality of second switches each connected between an input of one of said voltage followers and an output of one of said first switches,

wherein said first switches are turned ON for a first predetermined time period, and then, said second switches are turned ON while said first switches are turned OFF.

27. The apparatus as set forth in claim 26, wherein said

output circuit further comprises a plurality of third switches each connected between the output of one of said first switches and a ground, said third switches being turned ON by a control signal when driving of one of said display units is switched to driving of the other of said display unit.

28. The apparatus as set forth in claim 24, wherein each of said data driver circuits comprises:

a shift register circuit for shifting a horizontal start signal in accordance with a horizontal clock signal;

a line memory, connected to said shift register circuit, for storing one line data of said frame memory;

a gradation voltage generating circuit;

a decoder circuit, connected to said line memory and said gradation voltage generating circuit, for selecting gradation voltages from said gradation voltage generating circuit in accordance with output signals of said line memory; and

an output circuit, connected to said decoder, for outputting said selected gradation voltages, so that said selected gradation voltages are transmitted to the data lines of one of said display units.

29. The apparatus as set forth in claim 28, wherein said output circuit comprises:

a plurality of voltage followers, connected to said decoder circuit, for amplifying said selected gradation voltages;

a plurality of first switches each connected to one of said voltage followers; and

a plurality of second s witches each connected between an input of one of said voltage followers and an output of one of said first switches,

wherein said first switches are turned ON for a first predetermined time period, and then, said second switches are turned ON while said first switches are turned OFF.

30. The apparatus as set forth in claim 29, wherein said output circuit further comprises a plurality of third switches each connected between the output of one of said first switches and a ground, said third switches being turned ON by a control signal when driving of one of said display units is switched to driving of the other of said display unit.

31. The apparatus as set forth in claim 24, wherein said scan driver circuit comprises:

a shift register circuit for shifting a vertical start signal in accordance with a vertical clock signal; and

an output circuit, connected to said shift register circuit, for transmitting output signals of said shift register circuit to said second switch groups, so that the scan lines of one of said display units are sequentially scanned by said first switch groups.

32. The apparatus as set forth in claim 24, wherein said scan driver circuit further includes a plurality of second switch groups each second switch group being connected to the scan lines of said display units for supplying an off-level voltage to the scan lines of said one of said display units.

33. The apparatus as set forth in claim 24, further comprising:

an oscillator;

a plurality of first frequency dividers, connected to said oscillator, for frequency-dividing an output signal of said oscillator to generate horizontal clock signals;

a third switch group connected to said first

frequency dividers;

a plurality of second frequency dividers, connected to said oscillator, for frequency-dividing the output signal of said oscillator to generate vertical clock signals;

a fourth switch group connected to said second frequency dividers; and

a frequency control circuit, connected to said third and fourth switch groups, for selecting and turning ON one switch of said third switch group and one switch of said fourth switch group, so that the data lines of said one of said display units are driven by a selected one of said horizontal clock signals and the scan lines of said one of said display units are driven by a selected one of said vertical clock signals, thus always realizing a definite frame frequency of said one of said display units.